Efficiency-wise Optimal Design Methodology of LCLC Converter for Wide Input Voltage Range Applications

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Abstract— LCLC converter is an LLC-based, four-element resonant topology, which has been proved to achieve high voltage gain and high efficiency. Such trait makes LCLC converter specifically suitable for wide-input-voltage-range DC/DC applications. Currently, LCLC converter lacks a design method targeting at optimal efficiency over a wide input voltage range. In fact, due to the complexity, efficiency itself is seldom used as optimization criterion even for LLC designs. In this paper, a systematic methodology is proposed to optimize the efficiency at different input voltage levels for LCLC converter. Three mathematical programs (developed in MATLAB) are employed respectively to find all resonant parameter combinations that critically achieve the required voltage gain; precisely analyze the current stress in time domain; and comprehensively calculate the losses in the power circuit including magnetic components. The programs will automatically generate the optimal parameter design with highest weighted efficiency at desired input voltage levels, as well as the magnetic components construction with specified types and sizes of core and conductor. Besides, this method can be extended to other topologies for wide voltage range applications. To verify the effectiveness of the proposed optimal design method, the function of the mathematical tools will be carefully explained in this paper; and a step-by-step design will be demonstrated as an example. Simulation will be included to verify the accuracy of the method.

Keywords— *LLC; wide input voltage range; high voltage gain; design method; high efficiency*

I. INTRODUCTION

Over decades, power converters evolve to reduce both loss and size. Frequency modulated resonant converters are widely acknowledged to achieve higher efficiency than PWM converters thanks to its inherent soft switching character. LLC converter attracts massive research and industry interest because of its high efficiency as well as low easy EMI design [1]. However, in practical, if the required input voltage range is wide, LLC topology becomes less attractive. Once LLC converter is designed to achieve high voltage gain, the circulating magnetizing current in the resonant tank will be high. The high circulating current does not contribute to the load power, and will cause degradation of efficiency.

Some research has been conducted to modify LLC topology for wide input voltage range applications [2]-[6]. By using two phases or switching between half bridge and full bridge, the input voltage range of LLC converter can be extended. In addition to these methods, LCLC converter has been verified to achieve high voltage gain while maintain high overall efficiency [7]. As compared to conventional LLC converter, only one capacitor is added. Besides, conventional frequency modulation is still used in LCLC converter, which indicates high reliability and easy control.

For the parameter design, the prevailing method is empirical based design method. The designer needs to choose proper inductor ratio K and quality factor Q to achieve specified voltage gain. This method results in quick design but highly relies on the designers' experience to the application and requirement. The KQ method might be good for preliminary design, but not for optimization, which emphasizes on accuracy. To optimize an LLC converter for high efficiency, analysis based on time domain model is preferred over conventional FHA method due to the improved accuracy. Besides, most of the existing optimizing methods use current stresses rather than efficiency itself as the criterion for optimization. In these methods, it is assumed that the set of resonant parameters that achieves lowest current stress will result in the highest efficiency. This logic is flawed, since the magnetic components fabrication should also be taken into account for the final efficiency.

The logic of the efficiency-wise optimal design proposed in this paper is straightforward: the designers should find all possible parameter designs, power train components selection and magnetic components construction design; then calculate out the final loss of each design; and simply pick the design with the lowest loss as the optimal. The designer could use this design logic from scratch. Or use the proposed design method

after preliminary LLC parameter design with the empirical based design methods.

In order to calculate out the final efficiency accurately, steady-state analysis should be used to find the circuit model in time-domain [8], [9]. Numerical calculation software need to be used, because LLC converter's nonlinear behavior has no closed-form solution [10]. Besides, comprehensive loss model is needed to improve accuracy. These math tools lay the foundation of optimization.

In this paper, an optimal design methodology for LCLC converter operating over a wide input voltage range is proposed and exampled. This methodology is not limited to LCLC converter, and can be used on LLC converter and extended to all resonant converters and PWM converters in wide input voltage range applications. The optimization is based on weighted efficiency for desired input voltage levels. The content in this paper is arranged as the following: Section II explains the principle of LCLC converter achieving high gain. Section III introduces the mathematical tools and the optimization procedure. Section IV demonstrates a step by step design example of LCLC converter. Section V presents PSIM simulation verification and Section VI concludes the paper.

II. LCLC COVERTER OPERATION PRINCIPLE TO ACHIEVE HIGH VOLTAGE GAIN

The LCLC converter is shown in Fig. 1. A capacitor is connected in series with the parallel inductor, such that when the switching frequency reduces, the impedance on the parallel branch reduces more quickly as compared with that of the LLC converter. As a result, LCLC converter achieves higher gain than conventional LLC converter at low frequency (low input voltage). The detailed analysis will be given below.
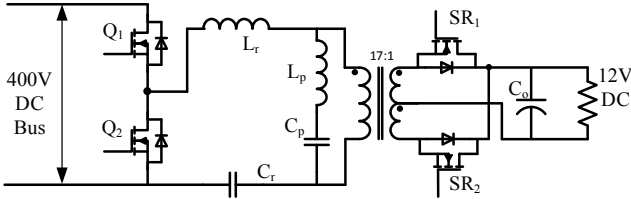

Fig. 1. LCLC converter topology

It is well known that the magnetizing inductance Lm is a crucial determinant for the peak voltage gain design of an LLC converter. According to First Harmonics Approximation (FHA) method, for given Lr and Cr, smaller Lm will result in higher voltage gain. In LCLC converter, the total impedance of Lp and Cp branch will remain inductive throughout the operating frequency range, such that LCLC converter can be equivalent an LLC converter with certain magnetizing inductor at given switching frequency. The equivalent Lm can be calculated by (1).

$$L_{m\_eq}\left(f_s\right) = L_p - \frac{1}{\left(2\pi f_s\right)^2 C_p} \tag{1}$$

When the input voltage drops, the switching frequency will reduce according to frequency modulation, thus the equivalent magnetizing inductor Lm_eq will reduce according to (1).   0 illustrates the relationship between Lm_eq and the operating frequency fs, using the parameters in TABLE I.

TABLE I.   PARAMETER OF LCLC CONVERTER

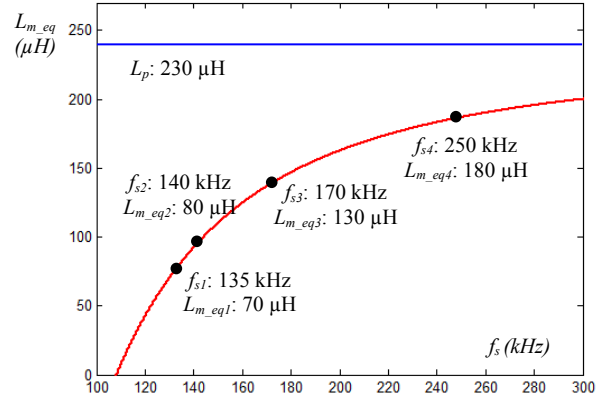| Lr (µH)	Cr (nF)	Lp (µH)	Cp (nF)
16	24	230	10

Fig. 2. Equivalent Lm changing with fs

As explained, if the magnetizing inductor is reduced, the voltage gain will be increased. Thus, at lower input voltage, the switching frequency will be lower, and the equivalent magnetizing inductor will be reduced, thus the higher peak gain can be achieved. The mathematical expression of the voltage gain of LCLC converter is shown in (2). And Fig. 3 shows the gain curves of the LCLC converter and its equivalent LLC converters.

$$G = \frac{1}{\sqrt{\left(1 + \frac{L_r}{L_{m\_eq}} - \frac{L_r}{L_{m\_eq}}\left(\frac{f_r}{f_s}\right)^2\right)^2 + \left(\frac{\pi^2}{8n^2}Q\left(\frac{f_s}{f_r} - \frac{f_r}{f_s}\right)\right)^2}} \tag{2}$$
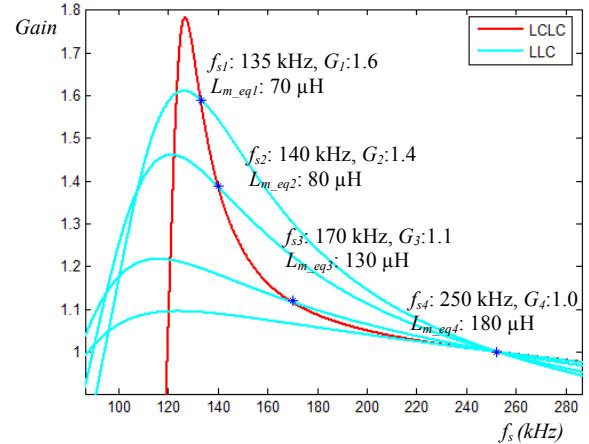

Fig. 3. LCLC and equivalent LLC gain curves

III. Effciency-wise Design Methodology of LCLC Converter for Wide Input Voltage Range

In this section, the criteria and logic of the optimal design will be explained. The mathematic tools used will be introduced. And the detailed design procedure will be presented in steps.

A. Criteria of optimization

As explained in Section I, to achieve optimal design of LCLC converter for wide input voltage range is to obtain the LCLC resonant parameter design (inductor and capacitor values) and magnetics fabrication (cores, wires, air gaps) that achieves highest weighted efficiency for desired input voltage levels. The weighted efficiency is defined in (3), in which V_{in_n} represents the input voltage levels at which the designer wants to optimize, and k_n is the coefficient (or the weight) constrained from 0 to 1. The motivation for weighing at different input voltage levels is that the converter may operate for long time at one input level but short at another. The number of input voltage levels interested and the weight of each level vary according to the designer's will. For simplicity, this paper considers 250 V and 400 V (two ends) efficiency with 50% weight each.

$$\eta_{wtd} = \sum_{n=1}^{N} k_n \cdot \eta_{V_{in\_n}} \left(\sum_{n=1}^{N} k_n = 1, k_n \in [0,1] \right) \quad (3)$$

B. Design logic

From the stand of system level design, the key of the proposed optimal design methodology is to find all possible LCLC resonant parameter designs candidates that meet the specified gain requirement at specified minimum frequency; and traverse all possible fabrications of inductor and transformer in each LCLC design candidate with specified cores and wires; then calculate total loss at 250 V and 400 V respectively, and choose the candidate with the lowest weighted loss. It is reasonable to determine the minimum frequency before the design, because minimum frequency usually determines core sizes, and size is usually prior to parameter design.

For each LCLC candidate, according to Fig. 3, once the parameters design are complete, 250V equivalent magnetizing inductor value Lm_250 and 400V equivalent Lm_400 value will respectively be appointed as the lower boundary and higher boundary of all equivalent magnetizing inductors over the entire frequency range. Thus, it is crucial to identify these two values. Excessively small Lm_250 will result in overdesign in terms of peak gain, while too large Lm_400 will sacrifice the room of ZVS operation for HB FETs. Neither of these two situations is acceptable from the point of view of increasing the efficiency.

The design logic of each LCLC candidate is: firstly designing the parameters of 250 V equivalent LLC converter achieving the exact peak gain at specified frequency; then designing 400 V equivalent LLC converter with same Lr and Cr; and in the end interpreting Lm_250 and Lm_400 with Lp and Cp. More details will explained in the following part.

C. Math tools

The optimal design method involves three important math tools: 1. peak gain solver; 2. magnetics designer; 3. loss analyzer. In this paper, the three tools are coded within MATLAB environment, and can be ported to other software environment with numerical calculation.

Peak gain solver is an accurate algorithm that finds all possible LLC design candidates achieving exactly the specified peak gain at specified minimum switching frequency. The algorithm is based on LLC time domain model at the critical inductive and capacitive boundary frequency (peak gain point of frequency modulation). At the peak gain point, the two possible operation modes – PN mode and PON mode have been well studied and described with equation sets for the component stress as well as timing. The algorithm will take traversal of all usable capacitor values in fixed incremental steps, and find out the according resonant inductor and magnetizing inductor which fit the time domain equation sets of either PN mode or PON mode. Once the parameter design is obtained, the components stresses such as current stress at a specific time instant and the flux in the transformer core *etc.* can calculated with the time domain model at arbitrary input and load condition. More details on the algorithm could be found in [11] and [12]. In this paper, the peak gain solver will be used to design the parameters of 250 V equivalent LLC converter.

Magnetics designer is an algorithm that finds all inductor design of specified inductor value and current stresses. The algorithm searches all design combinations with listed cores and conductors including litz wire and copper foil. For a specific core, the algorithm will take traversal of all available conductor to fit in the core with fixed increment of turns, and find the air gap accordingly. The algorithm will eliminate the impractical designs based on the predefined window utilization factor, maximum temperature rise, maximum air gap, maximum current density *etc.*. The core loss is then calculated by Steinmetz's equation [13]. In this paper, round litz wire is used as the conductor for inductors, and the copper loss can be calculated by Dowell's equation [14]. The design of transformer is similar.

Loss analyzer is an algorithm that summarizes the desired types of losses. The losses considered in this paper include switching and conduction loss of HB and SR FETs, core and winding loss of inductors and transformer. Other minor losses such as capacitor ESR loss, PCB track loss *etc.* could also be included. The more comprehensive the losses are covered, the more accurate will be the decision. For each LCLC candidate, the current waveform will be obtained immediately the parameter design is done. Thus the conduction losses calculation will be straightforward, and the accuracy is easy to verify by simulation. With the time domain analysis, the current and voltage information at the switching instant could

also be collected for the switching loss calculation. The accuracy of switching loss prediction will depend on the physical model of the switching behavior [15], [16]. Combining with the calculated core losses and copper loss in the inductors and the transformer, the converter efficiency at arbitrary input and load conditions could be obtained. Then the weighted efficiency could be estimated to evaluate each LCLC design candidate.

D. Detailed design procedure

Fig. 4 shows the optimal design flow chart. The detailed design procedure is presented below:

Design requirements:
input/output voltage, power, size

Design specification:
magnetic cores, minimum switching frequency, turns ratio, HB FETs, SR FETs, capacitors

Peak gain solver

LLC$_{250}$ #1: L$_{r1}$, C$_{r1}$, L$_{m\_250\_1}$
LLC$_{250}$ #2: L$_{r2}$, C$_{r2}$, L$_{m\_250\_2}$
LLC$_{250}$ #N: L$_{rN}$, C$_{rN}$, L$_{m\_250\_N}$

? ZVS @ 400V

LLC$_{400}$ #1: L$_{r1}$, C$_{r1}$, L$_{m\_400\_1}$
LLC$_{400}$ #2: L$_{r2}$, C$_{r2}$, L$_{m\_400\_2}$
LLC$_{400}$ #N: L$_{rN}$, C$_{rN}$, L$_{m\_400\_N}$

LCLC #1: L$_{r1}$, C$_{r1}$, L$_{p1}$, C$_{p1}$
LCLC #2: L$_{r2}$, C$_{r2}$, L$_{p2}$, C$_{p2}$
LCLC #N: L$_{rN}$, C$_{rN}$, L$_{pN}$, C$_{pN}$

Magnetics designer

LCLC #1_1: L$_{r1\_1}$, L$_{p1\_1}$, T$_{x1\_1}$
LCLC #1_2: L$_{r1\_2}$, L$_{p1\_2}$, T$_{x1\_2}$
LCLC #1_m: L$_{r1\_m}$, L$_{p1\_m}$, T$_{x1\_m}$

LCLC #2_1
LCLC #2_2
LCLC #2_m

LCLC #N_m
LCLC #N_m
LCLC #N_m

? Min loss @ 250V

LCLC #1 _optimal
LCLC #2 _optimal
LCLC #N _optimal

Loss analyzer

LCLC_optimal:
L$_r$ (value, make), L$_p$ (value, make), T$_x$ (make), C$_r$, C$_p$, $\eta_{\_estimate}$
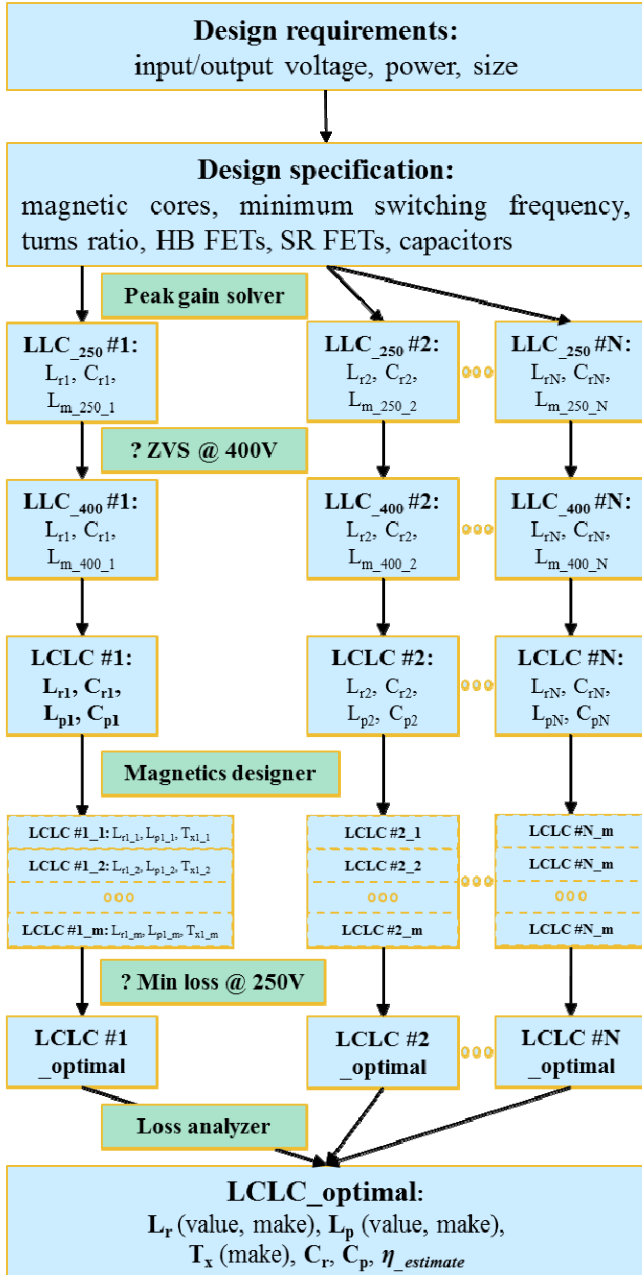
Fig. 4. Optimal design flow chart

1.   Specify design requirement including input and output voltages, power, and converter size *etc.*.

2.   Select discrete components including HB and SR MOSFETs, usable cores, wires, transformer turns ratios, and minimum switching frequency.

3.   Use the peak gain solver tool to design the resonant parameters of 250 V equivalent LLC converters at rated load.

Suppose total *N* sets of LLC_250 parameter design is obtained. Each design will contain the parameter of Lr, Cr, Lm_250.

4.   Use same Lr and Cr, and search for maximum value of Lm to achieve ZVS for HB switches for 400V operation. Record the value as Lm_400.

5.   Converter Lm_250 and Lm_400 to Lp and Cp.

6.   Determine the construction of Lr and Lp for candidate #1 with magnetics designer tool. Suppose total m sets of different making method are resulted. Mark the parameter design and magnetic design as LCLC candidate #1.1, candidate #1.2, … candidate #1.m.

7.   Repeat 6 for candidate #2 to candidate #N.

8.   Calculate converter loss with loss analyzer tool for 250V and 400V respectively. One with lowest weighted loss will be the optimal design for 250 V – 400 V LCLC converter. Until now, resonant parameters and magnetic components design and estimated efficiency are obtained.

IV.   AN LCLC CONVERTER DESIGN EXAMPLE WITH THE PROPOSED DESIGN METHODOLOGY

In this section, a step-by-step design example of LCLC converter will be used to explain the proposed optimal design methodology.

A. Specify requirements

The fundamental design requirements is shown in TABLE II. In the target application, the converter will occasionally operate at 250 V and 400 V input with same chance. Thus the weight for 250 V and 400 V are selected as $k_{250} = k_{400} = 0.5$.

TABLE II.   DESIGN REQUIREMENT OF LCLC CONVERTER

Input voltage	250 V – 400 V
Output voltage	12 V
Output power	500 W
Lr core	PQ 32/20
Lp core	PQ 32/30
Tx core	PQ 40/40

The magnetic components are usually a crucial factor for the converter size. Thus, the cores are usually listed as design requirement from the size point of view. In this paper, for simplicity, the cores for the resonant inductor Lr, parallel inductor Lp and the transformer Tx are predetermined as shown in TABLE II. In the setting of this design methodology, the designer could list as many cores as wished, and compare

the final efficiency. In the real world, however, designers might want to shrink the searching range with one or several specific cores for each of the inductor or transformer, such that the time cost could be reduced.

B. Design specification and component selection

TABLE III. shows the design specifications and the components selection.

The transformer turns ratio is determined based on the output voltage 12 V and the upper limit of the input voltage 400 V, and thus chosen at 16:1. The peak voltage gain required will be Gpk = 400 V / 250 V = 1.6. In real world design, taking into consideration of the conversion loss, the output power is encouraged to be set a little higher than the rated during the calculation. The output power used in this example is 520 W, which indicates the conversion efficiency is ~96%.

TABLE III.   DESIGN SPECIFICATION OF LCLC CONVERTER

Transformer turns ratio		16:1
Peak voltage gain		1.6
Output power used		520 W
Minimum frequency		150 kHz
Core material		3C95
SR MOSFET Rdson		1 mΩ
HB MOSFET	Rdson	110 mΩ
	tf	6 ns
	Coss	500 pF

When the core types are selected, the minimum switching frequency is also roughly determined, since operation at the minimum switching frequency will be the worst case of the magnetic components in terms of core loss and copper loss. In this paper, the minimum switching frequency is set at 150 kHz according to the cores selected. It should be noted that, in the setting of this design methodology, the designer could use a few different minimum switching frequencies, and compare the total results to reach the final decision.

As explained, the minimum switching frequency will be the worst case of core loss. Thus, the material could be selected based on the minimum switching frequency. 3C95 is used in this paper for simplicity. The designer could list as many materials as possible if a comprehensive comparison is desired.

The switches should be selected according to the specific design. The parameters of the SR FETs and the HB FETs selected in this paper are shown in TABLE III. The parameter Rdson is used to calculate the conduction loss. The parameter tf is the turn off time of the MOSFET, and will be used to calculate the turn off loss. The parameter Coss is the output capacitor, and will be used to calculate the turn on loss, if strict ZVS is not achieved.

C. 250V equivalent LLC design

Use the peak gain solver algorithm to solve the time domain equation. The results are listed in TABLE IV. The list has covered all combination of the resonant tank design which

achieves 1.6 as peak gain at the specified minimum switching frequency 150 kHz under rated 500 W.

The incremental step of Cr used in this example is 3nF. Using finer step of Cr would result in more design candidates. For example, if the Cr value is changing with 1nF every step, total 19 sets of LLC parameter will be generated by the algorithm. 3nF is used here as a coarse filter to roughly locate the optimal design. Designer could do a finer search near the coarse optimal design with the algorithm, if more accurate result is desired.

TABLE IV.   DESIGN CANDIDATES FOR 250V EQUIVALENT CONVERTER

Desgin No.	Cr (nF)	Lr (µH)	Lm_250 (µH)	fmin (kHz)
1	6	155	61	150
2	9	91	64	150
3	12	59	67	150
4	15	39	71	150
5	18	25	74	150
6	21	14	76	150

At this step, the designer could rule out part of the design candidates (shaded in TABLE IV.) based on engineering experience. For example, design No. 1 to design No. 3 seems odd, as the Lr value is similar or even bigger than the Lm value. According to the conventional KQ design, the inductor ratio K is usually chosen as 3 - 6, which means Lm should be 3 times the value of Lr.

D. 400V equivalent LLC design

The parameter of 400 V equivalent design will use the same Lr and Cr value in each of the 250V equivalent LLC parameters, while the Lm value will be increased, such that the circulating current near the resonant frequency could be reduced. Theoretically the Lm could be infinite, as the required gain for 400V is unity. However, in practice, the 400V equivalent magnetizing inductor Lm_400 should be properly designed so that ZVS could be achieved for the HB switches. TABLE V. summarizes the 400V equivalent LLC parameters, with which the converter achieves critical ZVS.

TABLE V.   DESIGN CANDIDATES FOR 400V EQUIVALENT CONVERTER

Desgin No.	Cr (nF)	Lr (µH)	Lm_400 (µH)	fr (kHz)
4	15	39	210	208
5	18	25	190	237
6	21	14	150	289

Besides, smaller value than the suggested 400V equivalent Lm in TABLE V. could also be used, as long as it is larger than Lm_250 for each LLC candidate. Designers could reduce the Lm_400 value with desired steps and calculate out the final efficiency to make the whole design more comprehensive.

E. LCLC parameter from equivalent 250V and 400V design

From resonant parameter of 250V and 400V equivalent LLC design, a unique set of Lp and Cp value can be found,

whose combined impedance is same with Lm_400 at fr and same with Lm_250 at fmin. Lp and Cp of each LCLC candidate could be calculated with the equation set in (4).

$$
\begin{cases}
L_p = \dfrac{f_r^2 L_{m\_400} - f_{min}^2 L_{m\_250}}{f_r^2 - f_{min}^2} \\[4mm]
C_p = \dfrac{f_r^2 - f_{min}^2}{\left(2\pi f_r f_{min}\right)^2 \left(L_{m\_400} - L_{m\_250}\right)}
\end{cases}
\tag{4}
$$

When the Lp and Cp is obtained, the voltage stress on Cp for 250 V (worst case) could also be calculated in the time domain model. Or it could also be estimated by FHA. The reflected ac voltage v_{ac} across the transformer is known, and Lp and Cp become a voltage divider circuit. The peak voltage stress can be calculated in (5).

$$
v_{Cp\_pk} = \frac{v_{ac}}{Z_{Lp}} Z_{Cp} = \frac{\frac{4}{\pi} N V_o}{2\pi f_{min} L_p} \frac{1}{2\pi f_{min} C_p}
\tag{5}
$$

TABLE VI. summarizes the parameter design of LCLC candidates based on the 250V and 400V equivalent LLC design.In this step, part of the design candidates could be ruled out if the Cp voltage is not practical. For example, the DC voltage rating of the film capacitor in this design is 1000 V, and the peak voltage on Cp exceeds this limit in design No. 4 (shaded in TABLE VI.).

F. Time domain analysis of the equivalent LLCs at different input voltage

In this step, the parameter designs resulted previously will be used to calculate the current stresses in time domain model for both 250V and 400V. If the efficiency at other input voltage is also involved, the current stress at that voltage should also be calculated at this step.

The current stress analysis is summarized in TABLE VII. and TABLE VIII. for 250V input and 400V input respectively. iLr_tf is the resonant current at the turn off instant, which will be used to calculate the turn off loss. iLr_rms and iLp_rms are the RMS value of the resonant current and the current on parallel branch, which will be used for copper loss calculation. iLr_pk and iLp_pk are the peak value of the resonant current and the current on parallel branch, which will be used to calculate the core loss. isec_rms will be used to calculate the conduction loss in SR.

G. Magnetic design

Use the inductor designer tool to design the inductor in each of the LCLC candidates.

Taking the resonant inductor in LCLC design No. 6 in TABLE VI. as an example, the inductor value is 14 μH. The core for Lr has been specified in the first step as PQ 32/20

(3C95). At worst case 250V, the peak current stress is 4.41A, and the RMS current is 3.09A (shown in TABLE VII.). By inputting the Lr value, iLr_pk value and iLr_rms value, the design algorithm results are shown in TABLE IX. It could be observed that with fewer turns, the inductor has lower copper loss but high core loss. If the turns count is increased to 10, finer litz wire needs to be used due to the limited window size. Comparing the 5 inductor candidates, it is found that the construction of 9 turns with ~1.8 mm air gap is the optimal design for 250V. And it will be used as the inductor design for the LCLC converter. In practice, the designer could compare the inductor design at 400V also if it is wished.

Similarly, the inductor and transformer in other LCLC candidates could be designed with the tool.

H. Loss comparison

Use the loss analyzer tool to calculate and summarize the total loss on the magnetic components and switches on both primary side and secondary side.

The results are shown in TABLE X. and TABLE XI. for 250V operation and 400V operation respectively. Comparing design No. 5 and No. 6, it is observed that design No. 6 has lower loss at 250V and higher loss at 400V. Put the efficiency at 250V and 400V into (3) for each of the LCLC candidates, and the weighted efficiency could be obtained. As it is assumed that 250V operation has the same weight as 400V, it is found that LCLC design No.6 has higher weighted efficiency at 97.9% than that of No.5 design at 97.8%.

If the design requirement tends to emphasize 400V efficiency, then design No.5 will be better choice than No.6.

Designer could conduct a finer search around the optimal design in the further step, if more accurate result is desired.

V. SIMULATION VERFICATION

The specifications of parameter design of LCLC converter is shown in TABLE XII. The two design results No.5 and No. 5 will be compared in PSIM simulation of current stresses at both 400V and 250V input condition.

TABLE XII   SPECIFICATIONS OF LCLC CONVERTERS

Input voltage	250 V – 400 V	
Output voltage/power	12 V / 500 W	
Transformer turns ratio	16:1	
Design No.	No. 5	No. 6
Resonant inductor	25μH	14μH
Resonant capacitor	18nF	21nF
Parallel inductor	300μH	186μH
Parallel capacitor	4.2nF	8.6nF

Fig. 5 shows the current waveform at 250V for Design No. 5. The current stress are displayed with the error in percentages as compared to the data shown in TABLE VII.

Fig. 6 shows the current waveform at 400V for Design No. 5. The error of current stress are compared with TABLE VIII.

Desgin No.	Cr (nF)	Lr (μH)	Lp (μH)	Cp (nF)	fr (kHz)	fmin (kHz)	VCp_pk (V)
4	15	39	430	2.7	208	150	1300
5	18	25	300	4.2	237	150	740
6	21	14	186	8.6	289	150	310

Desgin No.	Cr (nF)	Lr (μH)	Lp (μH)	Cp (nF)	Lm_250 (μH)	fmin (kHz)	iLr_tf (A)	iLr_rms (A)	iLr_pk (A)	iLp_rms (A)	iLp_pk (A)	Isec_rms (A)
5	18	25	300	4.2	74	150	1.99	4.59	7.34	2.26	3.41	55.3
6	21	14	186	8.6	76	150	1.43	4.72	8.33	1.93	2.83	61.3

Desgin No.	Cr (nF)	Lr (μH)	Lp (μH)	Cp (nF)	Lm_400 (μH)	fmin (kHz)	iLr_tf (A)	iLr_rms (A)	iLr_pk (A)	iLp_rms (A)	iLp_pk (A)	Isec_rms (A)
5	18	25	300	4.2	190	237	1.14	2.98	4.23	0.86	1.14	44.5
6	21	14	186	8.6	150	289	1.13	3.09	4.41	0.87	1.15	45.7

Core size	Material	Turns	Air gap	Litz_AWG	Strands	Core loss	Winding loss	Total loss
PQ 32/20	3C95	6 turns	0.70 mm	42 AWG	165 stands	3.62	0.22	3.85
PQ 32/20	3C95	7 turns	0.99 mm	42 AWG	165 stands	2.29	0.29	2.59
PQ 32/20	3C95	8 turns	1.35 mm	42 AWG	165 stands	1.57	0.40	1.98
PQ 32/20	3C95	9 turns	1.79 mm	42 AWG	165 stands	1.10	0.69	1.79
PQ 32/20	3C95	10 turns	2.35 mm	42 AWG	105 stands	0.79	1.12	1.92

Design No.	Lp (PQ 32/30)			Lr (PQ 32/20)			Tx (PQ 40/40)				HB_FETs				SR		Total 400V
	core	copper	total	core	copper	total	core	copper_1st	copper_2rd	total	ON	turnoff	Coss	total	Rdson	total	
5	0.33	0.26	0.60	0.45	0.50	0.95	0.10	0.22	0.52	0.85	0.97	0.80	0	1.77	2.57	2.57	6.76
6	0.20	0.23	0.44	0.35	0.38	0.74	0.17	0.27	0.70	1.16	1.05	0.96	0	2.02	2.72	2.72	7.09

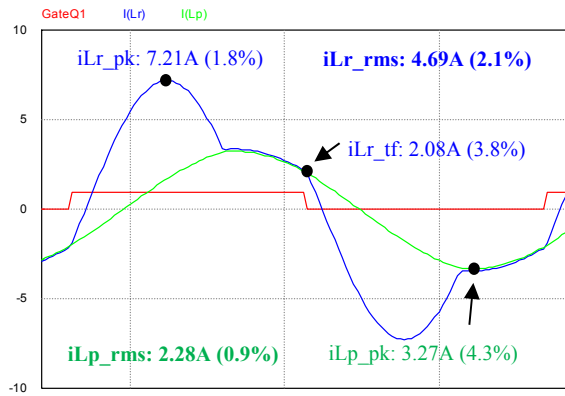| Design No.	Lp (PQ 32/30)			Lr (PQ 32/20)			Tx (PQ 40/40)				HB_FETs				SR		Total 250V
	core	copper	total	core	copper	total	core	copper_1st	copper_2rd	total	ON	turnoff	Coss	total	Rdson	total	
5	2.8	1.84	4.64	1.10	0.69	1.79	0.86	0.35	0.81	2.02	2.32	0.97	0	3.30	3.98	3.98	15.73
6	0.82	1.16	1.98	1.01	0.41	1.42	0.72	0.49	1.27	2.48	2.45	0.70	0.24	3.39	4.88	4.88	14.16

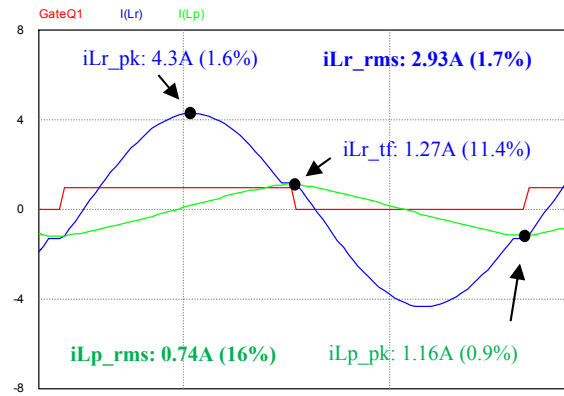Fig. 5. Current waveforms of Design No.5 at 250V input

Fig. 6. Current waveforms of Design No.5 at 400V input

Fig. 7 shows the current waveform at 250V for Design No. 6. The current stress are displayed with the error in percentages as compared to the data shown in TABLE VII.

As can be observed, the phase lag of the resonant current is smaller for No.6 at 250V than No.5 design, which corresponds to the calculated Coss loss in TABLE XI.
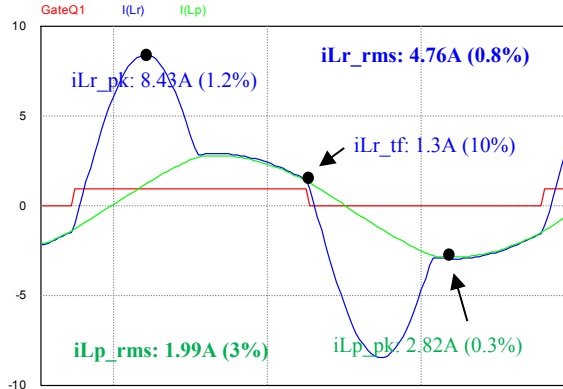

Fig. 7.   Current waveforms of Design No.6 at 250V input

Fig. 8 shows the current waveform at 400V for Design No. 6. The error of current stress are compared with TABLE VIII.
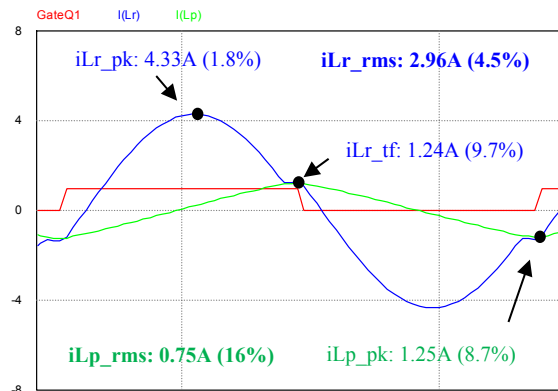

Fig. 8.   Current waveforms of Design No.6 at 400V input

Compared with the PSIM simulation, it is observed that very high accuracy of current stresses are resulted from the model and the calculation.

VI.   CONCLUSION

In this paper, a systematic design methodology is proposed to design LCLC converter to achieve optimal weighted efficiency for wide input voltage range. The design method is also suitable for LLC converter and other resonant converters aiming at wide input voltage range application. The design methodology is simple in logic and accurate for results, as it employed time domain model for current stress analysis. Besides, the design methodology involves both resonant parameter design and magnetic construction design. The mathematic tools used in the design method has been explained, and a step by step design example of LCLC converter has been presented to designer gain the insight of the proposed optimal design methodology. Comparisons of the current stresses of the calculation and PSIM simulation have been demonstrated, which verifies the high accuracy of the design results.

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